ABSTRACT

A cellular automaton cache memory architecture. On a general-purpose processor, a cache memory is provided to store instructions and data for use by the processor. The cache memory is further capable of storing data representing a first state of a cellular automaton at a first time step, where the data is organized in cells. A cellular automaton update unit provides data from selected cells of the cellular automaton to an update engine. The update engine updates at least some of the selected cells according to an update rule and a state of any associated neighborhood cells to provide a state of the cellular automaton at a second time step.

UNITED STATES PATENT AND TRADEMARK OFFICE
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Drawings

7

Level - 2
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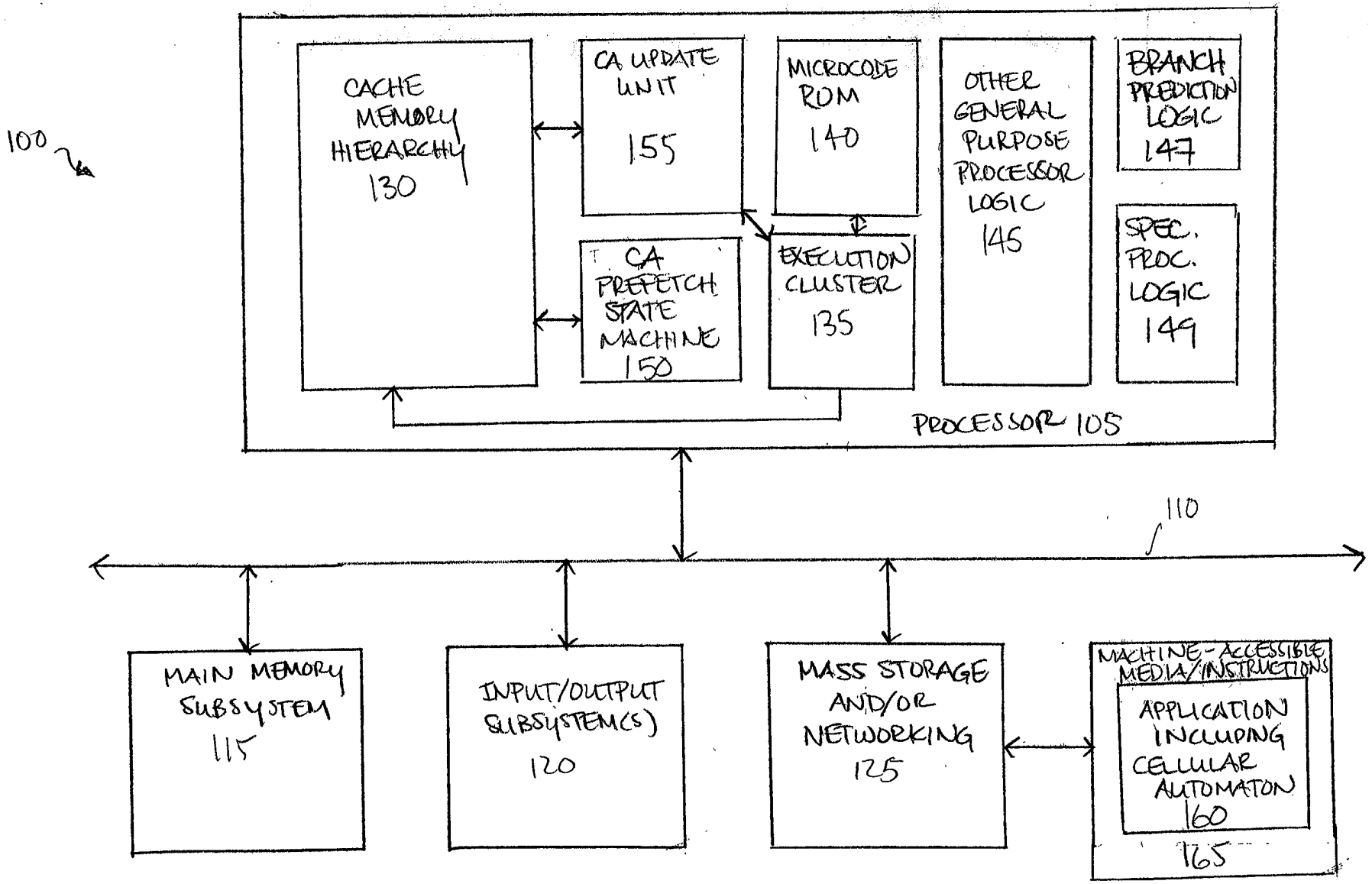

FIGURE 1

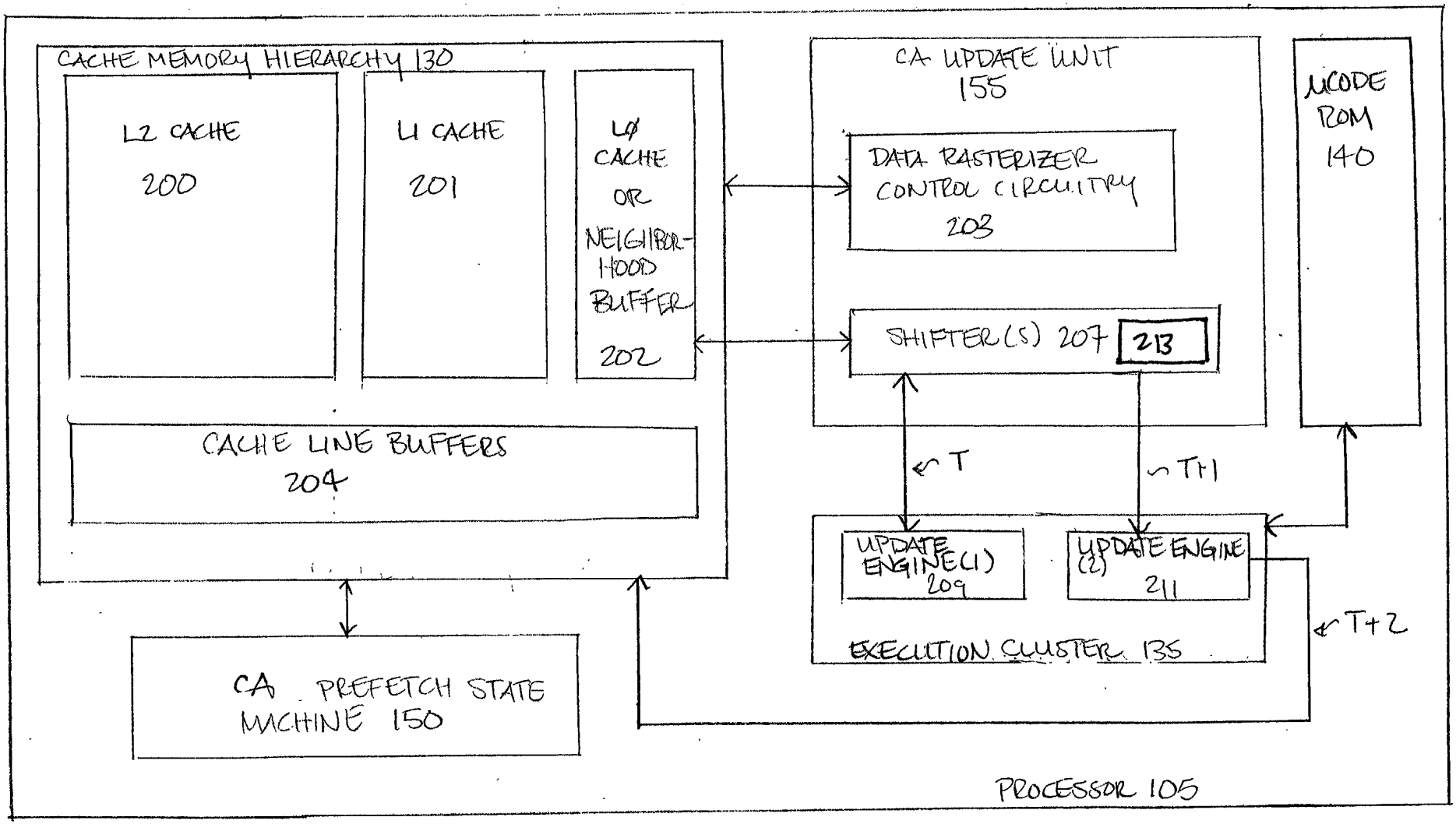
CACHE MEMORY HIERARCHY 130
L2 CACHE
200
L1 CACHE
201
L0 CACHE OR NEIGHBOR-HOOD BUFFER
202
CACHE LINE BUFFERS
204
CA PREFETCH STATE MACHINE 150
CA UPDATE UNIT
155
DATA RASTERIZER CONTROL CIRCUITRY
203
SHIFTER(S) 207
213
UCODE ROM
140
T
T+1
UPDATE ENGINE(1)
209
UPDATE ENGINE (2)
211
EXECUTION CLUSTER 135
T+2
PROCESSOR 105

FIGURE 2

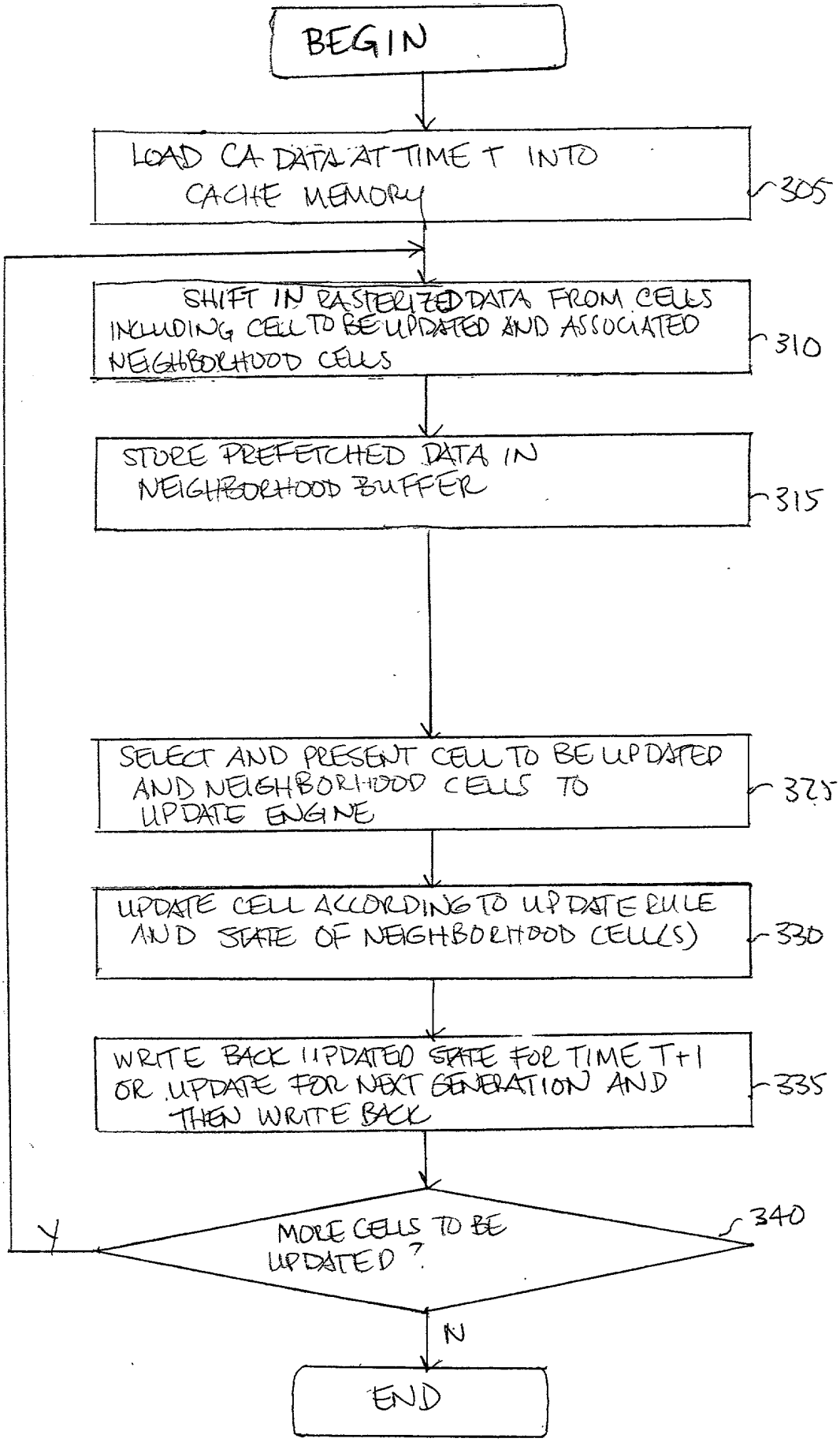
BEGIN
LOAD CA DATA AT TIME T INTO CACHE MEMORY
305
SHIFT IN RASTERIZED DATA FROM CELLS INCLUDING CELL TO BE UPDATED AND ASSOCIATED NEIGHBORHOOD CELLS
310
STORE PREFETCHED DATA IN NEIGHBORHOOD BUFFER
315
SELECT AND PRESENT CELL TO BE UPDATED AND NEIGHBORHOOD CELLS TO UPDATE ENGINE
325
UPDATE CELL ACCORDING TO UPDATE RULE AND STATE OF NEIGHBORHOOD CELL(S)
330
WRITE BACK UPDATED STATE FOR TIME T+1 OR UPDATE FOR NEXT GENERATION AND THEN WRITE BACK
335
MORE CELLS TO BE UPDATED ?
340
Y
N
END

FIGURE 3

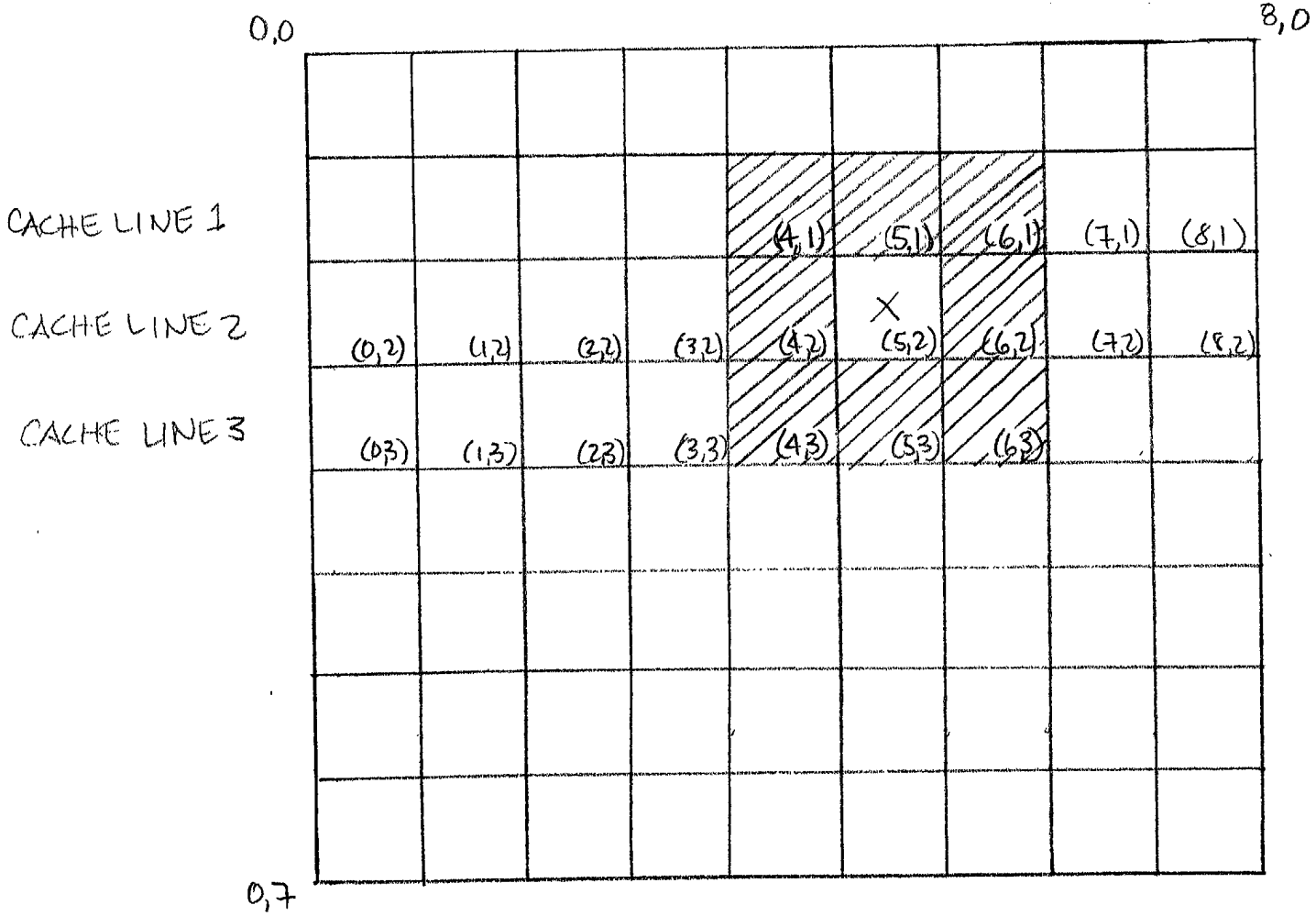

FIGURE 4

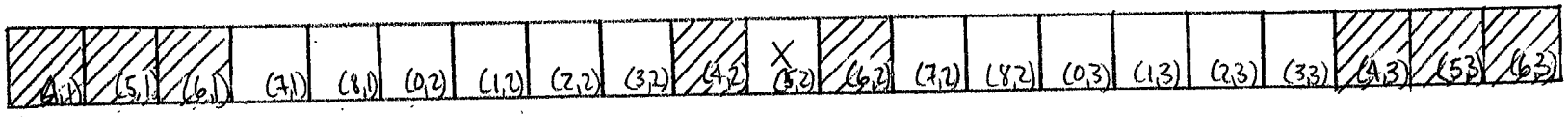

FIGURE 5